REMARKS

The Office Action notes that claims 1-9 are pending in the application. Of these, claims 4-9 were withdrawn from consideration subject to a restriction requirement. By this response, claim 1 has been amended. A portion of the amendment is formal in nature and the remaining portion is supported in the specification on page 11, lines 18-21. Therefore, no new matter has been added. Claims 1-9 remain pending with claims 1-3 under consideration.

Claims 1 and 3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kanamori (U.S. Patent No. 6,414,346).

Claim 1 as amended recites "a mask ROM." The mask ROM comprises:

> a substrate where a memory cell array region and a segment select region are defined;
>
> first and second trenches respectively formed at the outer portion of the memory cell array region and at the outer portion of a buried layer formation region of the segment select region;
>
> a first isolation film and an isolating pattern respectively filling up the first and second trenches, wherein the second isolating film isolates the segment select region from the memory cell array region;
>
> a plurality of buried layers aligned on the substrate in a first direction by a predetermined interval, and surrounded by the second isolation film; and
>
> a plurality of gates aligned in a second direction to cross the buried layers in an orthogonal direction.

To anticipate claim 1, the Office Action must establish that Kanamori discloses all of the elements of claim 1 as set forth therein. The Applicant respectfully submits that claim 1 is allowable over Kanamori because Kanamori does not teach or suggest all the elements of claim 1.

Referring to Fig. 5 of Kanamori, a semiconductor memory is provided that includes a memory cell region 2 and a peripheral circuit region 3. The memory cell region 2 spreads from the upper ends to the lower ends of element separating shield electrode 7. The peripheral circuit region spreads from the upper ends to the lower ends of element separation insulating films 9 (column 6, lines 59-65). The diffusion layers of first select transistors TRS 1, which are adjacent to each other in a row

direction, are subjected to element separation by the insulating films 9 (column 7, lines 50-53).

The Office Action equates separating insulation films 9 of Kanamori to the first and second trenches of claim 1. Claim 1, however, specifies that the second isolating film, which fills the second trench, isolates the segment select region from the memory cell array region. As can be seen from Figs. 5 and 8 of Kanamori, however, insulating films 9 do not separate memory cell region 2 and peripheral circuit region 3 but rather separate the diffusion layers of select transistors TS1, which are contained in peripheral circuit region 3 and run in a row direction. Accordingly, Kanamori does not disclose all of the features of claim 1 as set forth therein. The remaining claims are dependent on claim 1. Because dependent claims include the limitations of their base claim, dependent claims are not anticipated by Kanamori for the same reasons as given with respect to claim 1. Therefore, the applicant respectfully submits that all pending claims are in condition for allowance. Favorable reconsideration is hereby requested.

Respectfully submitted,

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I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

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